PATENT APPLICATION
DOCKET NO.: 1263-0009US

REMARKS

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Claims 1-20 are pending, of which claims 1 and 11 are in independent form. Claims 1, 4, 7-11, 14, and 15 are amended hereby. No new matter is introduced.

Regarding the Claim Rejections - 35 U.S.C. § 102

In the pending Office Action, independent claim 11 is rejected under 35 U.S.C. §102(b) as being anticipated by Jim Handy's *The Cache Memory Book*, 2nd Ed., pages 42-49 and 88-95 (hereinafter the *Handy* reference). The following comments were provided with respect to the §102 rejection:

> Handy discloses in Figure 2.4b a semiconductor memory circuit having a plurality of hierarchically organized levels, comprising the steps of:
>
> initiating a data access operation for accessing data in said semiconductor memory circuit (outward arrow from CPU on address line);
>
> determining if said data is available in a first level memory portion of said semiconductor memory circuit (arrow entering cache-tag);

> if not, accessing said data in a next level memory portion of said semiconductor memory circuit (arrow along address feeding through address buffer into main memory); and
>
> selectively loading said data accessed from said next level memory portion into said first level memory portion in a substantially simultaneous loading operation (arrows on data bus feeding cache data memory and CPU simultaneously).

Applicant respectfully submits that the pending §102 rejection has been overcome or otherwise rendered moot by the present response. The present invention as defined by the current base claim 11 is directed to a memory operation method for use in a semiconductor memory circuit having a plurality of hierarchically organized levels. Upon initiating a data access operation for accessing data in the semiconductor memory circuit, a determination is made if the data is available in a first level memory portion of the semiconductor memory circuit. If the data is not in the first level memory portion, a next level memory portion that is integrated within the semiconductor memory circuit is accessed. Data accessed from the next level memory portion is selectively loaded into the first level memory portion integrated therewith, in a loading operation that is

substantially simultaneous relative to the accessing of the data in the next level memory portion.

In contrast to the claimed invention, the *Handy* reference discloses a cache-based CPU-to-main-memory interface where four basic cache/CPU interaction modes are described as shown in Figures 2.4(a)-(d). Applicant respectfully asserts that the main memory and cache data memory components disclosed in the *Handy* reference, which are provided as discrete components separated by a system bus, do not teach, anticipate, or even remotely allude to the claimed first and next level memory portions that are integrated into a semiconductor memory circuit. Even if one were to equate the first level and next level memory portions with the cache data memory and main memory components, respectively, of the *Handy* reference, the "read miss" interaction shown in Figure 2.4(b), does not teach selective loading of data accessed from the next level memory portion into the first level memory portion in a loading operation that is substantially simultaneous relative to the accessing of the data in the next level memory portion. Applicant respectfully maintains that the arrangement of a data bus commonly feeding the cache memory and CPU in Figure 2.4(b) of the *Handy* reference does not teach or anticipate these

claimed limitations and, accordingly, claim 11 is believed to be in condition for allowance.

Regarding the Claim Rejections - 35 U.S.C. § 103

In the pending Office Action, claims 1-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the *Handy* reference in view of the U.S. Patent No. 6,675,265 to Barroso et al. (hereinafter the *Barroso* reference). The following comments were provided with particular reference to the §103(a) rejection of the base claim 1:

> In regards to claim 1, Handy discloses a semiconductor memory circuit having a plurality of hierarchically organized levels, comprising:
>
> a first level memory portion for storing data therein figure 2.23 L1 cache,
>
> a second level memory portion for storing data therein figure 2.23 L2 cache, and
>
> whereby data accessed from said second level memory portion is selectively loaded into said first level memory portion in a substantially simultaneous loading operation figure 2.4 arrows on data bus feeding cache data memory and CPU simultaneously.
>
> Handy does not disclose said first level memory portion having first level Data In (DIN) and Data Out (DOUT) buffer blocks associated therewith for effectuating data

operations with respect to a location in said first level memory portion, said first level DIN buffer block including Local Data In (LDIN) driver circuitry;

said second level memory portion having second level Data In (DIN) and Data Out (DOUT) buffer blocks associated therewith for effectuating data operations with respect to a location in said second level memory portion;

or a multiplexing circuitry disposed in said first level DIN buffer block, said multiplexing circuitry being actuatable for providing data accessed through said second level DOUT buffer block to said LDIN driver circuitry in said first level DIN buffer block.

Barroso discloses an example of the input and output buffers in figure 10c element 408, Barroso also discloses a multiplexor for selectively feeding the contents of the data out buffer to the L1 cache viz Mux element 416. It is well known in the art to use data in and data out buffers in conjunction with cache memory, especially in the case where the cache uses a single port memory, this is done to prevent the need for wait states when the cache in question is busy when a request is made. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate data input and output buffers with a cache memory and a multiplexor to feed data from L2 data output buffer to the L1 data input buffer.

In addition, dependent claims 12, 13 and 15-20 depending from the base claim 11 are also rejected under 35 U.S.C. §103(a) as being unpatentable over the *Handy* reference in view of common knowledge.

Applicant respectfully submits that the pending §103(a) rejections have been overcome or otherwise rendered moot by the present response. The present invention as currently defined involves a hierarchically organized semiconductor memory circuit and associated memory operation wherein data accessed from a higher level memory portion (e.g., a second level memory portion or a third level memory portion) is selectively loaded into a corresponding lower level memory portion (e.g., a first level memory portion or a second level memory portion) of the semiconductor memory circuit in a loading operation that is substantially simultaneous relative to the accessing of the data in the higher level memory portion. Appropriate multiplexing circuitry is included for actuating the corresponding Data In (DIN) driver circuitry in order to effectuate lower level loading operations while data from higher levels is being accessed.

As explained above, the *Handy* reference is deficient with respect to the claimed limitations. The *Barroso* reference, on the other hand, is of no avail in this regard. The *Barroso*

reference discloses a multiprocessor cache coherence system and method in which processor nodes and input/output nodes are treated as equal participants. As shown in Figure 10C, various data paths and components of an L2 cache 116 are illustrated wherein MUX 416 is operable for selecting between data stored in a temporary data buffer 408 and L2 cache data provided via a bypass path 410. See col. 20, lines 13 et seq. Applicant respectfully asserts that MUX operation of L2 cache 116 does not teach or suggest the claimed limitation of selectively loading data into a lower level memory portion, which data is being accessed from a higher level memory portion of the semiconductor memory circuit.

Based on the foregoing discussion, it is believed that the base claims 1 and 11 are allowable over the art of record. Additionally, dependent claims 2-4 depending from the base claim 1 and dependent claims 12, 13 and 15-20 depending from the base claim 11, which include all the limitations of the respective base claims, are also in condition for allowance for the same reasons set forth hereinabove.

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Regarding the Allowable Subject Matter

Applicant appreciates the indication in the outstanding Office Action that claims 5-10 and 14 would be allowable if rewritten in independent form including all of the limitations of the corresponding base claim and any intervening claims. In view of the present response, it is believed that the entire set of active claims, claims 1-20, are believed to be allowable in their current form.

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SUMMARY AND CONCLUSION

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding objections and rejections and allow claims 1-20 presented for reconsideration herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested.

Respectfully submitted,

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